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CERTIFICATION OF TRANSLATION

I, Byunghee Min, an employee of Y.P.LEE, MOCK & PARTNERS of The Cheonghwa Bldg., 1571-18 Seocho-dong, Seocho-gu, Seoul, Republic of Korea, hereby declare under penalty of perjury that I understand the Korean language and the English language; that I am fully capable of translating from Korean to English and vice versa; and that, to the best of my knowledge and belief, the statements in the English language in the attached translation of the priority document (Korean Patent Application No. 10-1997-0023917), consisting of 34 pages, have the same meanings as the statements in the Korean language in the original document, a copy of which I have examined.

Signed this 12 day of July, 2005

BYUNG HEE MIN

ABSTRACT

[Abstract of the Disclosure]

A method of manufacturing a semiconductor memory device that prevents oxidation of the bit lines caused by misalignment which may occur when patterning a storage electrode, and the semiconductor memory device. The method includes: forming a transistor including a gate, a source, and a drain in active regions of a semiconductor substrate; forming a pad connected to the source; forming a first insulating layer on the resultant structure having the pad; forming a plurality of bit lines connected to the drain on the first insulating layer; forming an oxidation preventing layer on the surface of the bit lines and the first insulating layer; forming a second insulating layer on the oxidation preventing layer; forming a contact hole exposing a portion of the semiconductor substrate; forming a spacer on inner sidewalls of the contact hole; forming a storage electrode connected to the pad via the contact hole; and sequentially forming a dielectric layer and a plate electrode on the storage electrode.

[Representative Drawing]

FIGS. 7, 8, 10, 11, and 12

SPECIFICATION

[Title of the Invention]

Method for manufacturing semiconductor memory device for preventing bit line oxidation and semiconductor memory device

[Brief Description of the Drawings]

FIG. 1 is a sectional view taken in a direction of a word line, for explaining a method for forming a conventional DRAM;

FIG. 2 is a sectional view showing a situation in which misalignment occurs during photolithography for forming a storage electrode;

FIG. 3 is a graph showing deposition characteristics of a nitride layer depending on the underlayer composition;

FIGS. 4 through 7 are sectional views for explaining a method of forming a semiconductor memory device according to a first embodiment of the present invention;

FIG. 8 is a sectional view for explaining a method of forming a semiconductor memory device according to a second embodiment of the present invention;

FIGS. 9 and 10 are sectional views for explaining a method of forming a semiconductor memory device according to a third embodiment of the present invention;

FIG. 11 is a sectional view for explaining a method of forming a semiconductor memory device according to a fourth embodiment of the present invention;

FIG. 12 is a sectional view for explaining a method of forming a semiconductor memory device according to a fifth embodiment of the present invention; and

FIG. 13 is a graph that compares the thicknesses of a nitride layer deposited on a BPSG layer depending on the surface processing used before depositing the nitride layer.

< Explanation of Reference numerals designating the Major Elements of the Drawings >

40: Field oxide layers	42: Pad
44, 52, 54, 56: Insulating layers	46: Polysilicon layer
48: Silicide layer	50, 70, 85, 90: Oxidation preventing layer
60, 75, 80: Spacer	62: Storage electrode
64: Dielectric layer	66: Plate electrode

[Detailed Description of the Invention]

[Object of the Invention]

[Technical Field of the Invention and Related Art prior to the Invention]

The present invention relates to a method for manufacturing a semiconductor device, and more particularly, to a method for manufacturing a semiconductor memory device that is resistant to oxidation of the bit lines.

In manufacturing a dynamic random access memory (DRAM), to increase the operational speed of a device, a bit line is generally formed by a polycide structure obtained by depositing an impurity-doped polysilicon and a low-resistance silicide.

FIG. 1 is a sectional view for explaining a method for manufacturing a conventional DRAM.

Referring to FIG. 1, a transistor (not shown) is formed by a conventional manner on a semiconductor substrate 100 divided into active regions (not shown) and field regions (not shown) by field oxide layers 12. Next, polysilicon is deposited on the resultant structure and then patterned, thereby forming a pad 14 for connecting a storage electrode to the active region (source region) of the semiconductor substrate 100. After the pad is formed, an insulating material is deposited on the resultant structure and then planarized, thereby forming a first insulating layer 16 for insulating the transistor from another conductive layer. To facilitate the planarization, the first insulating layer 16 may be formed of a fluid insulating layer, e.g., borophosphosilicate glass (BPSG) or undoped silicate glass (USG).

Next, a bit line contact (not shown) and bit line 18 and 20 is formed by a conventional method and then a planarized second insulating layer 22 is formed on the resultant structure. The bit line is formed by depositing a doped polysilicon layer 18 and a silicide layer 20 on the first insulating layer 16, and the second insulating layer 22 is formed in a similar manner to the first insulating layer 16. Subsequently, a nitride layer 24 and an oxide layer 26 are sequentially deposited on the resultant structure.

Next, the oxide layer 26, the nitride layer 24, the second insulating layer 22 and the first insulating layer 16 are anisotropically etched by photolithography to form a contact hole exposing the pad 14. A nitride layer is deposited on the surface of the resultant structure having the contact hole to form a spacer 28 on the sidewall of the

contact hole. The spacer 28 helps prevent the oxidation of the bit lines by oxygen diffused through the sidewall of the contact hole.

Next, a polysilicon layer is deposited on the resultant structure, and patterned by photolithography to form a storage electrode 30. A dielectric layer 32 and a plate electrode 34 are formed on the storage electrode 30 by a conventional method. The dielectric layer 32 may be formed in an NO structure obtained by depositing a nitride layer and by forming an oxide layer, for the purpose of improving capacitor characteristics. The nitride layer is typically formed by a chemical vapor deposition (CVD) method, and the oxide layer is formed by a thermal oxidation method. As semiconductor memory devices become highly integrated, misalignment may occur during the photolithography for forming the storage electrode 30.

FIG. 2 is a sectional view showing an example of such misalignment.

In FIG. 2, if misalignment occurs between the storage electrode 30 and the contact hole of the storage electrode 30, an overetch may occur on the nitride layer spacer 28 when the storage electrode 30 is patterned by etching. Accordingly, the second insulating layer 22 is exposed at the sidewall of the contact hole. If the second insulating layer 22 is exposed, the nitride layer is deposited more thinly on the exposed second insulating layer 22 than on other layers when the dielectric layer 32 is formed in a subsequent step. This phenomenon is caused by the different deposition rates of the nitride layer, depending on the composition of the underlayer, which is illustrated in FIG. 3.

FIG. 3 shows the deposition characteristics of the nitride layer for both a wafer

underlayer and a BPSG underlayer. In FIG. 3, "A" indicates the thickness of the nitride layer deposited on a bare wafer, and "B" indicates the thickness of the nitride layer deposited on a BPSG layer.

As shown in the graph for a deposition time of 50 minutes, when the nitride layer is deposited on the bare wafer to a thickness of about 50 angstroms, the nitride layer is deposited to be only 37 angstroms thick on the BPSG layer.

Therefore, as shown in FIG. 2, the second insulating layer 22 is susceptible to oxygen diffusion because the oxygen used during thermal oxidation in forming the oxide in the dielectric layer 34 may penetrate into a portion of second insulating layer 22 where the nitride layer is deposited thinly.

[Technical Goal of the Invention]

Therefore, an object of the present invention is to provide a method for manufacturing a semiconductor memory device which can prevent oxidation of a bit line.

[Structure and Operation of the Invention]

To accomplish the above object of the present invention, there is provided a method for manufacturing a semiconductor memory device including the steps of forming a transistor including a gate, a source, and a drain in active regions of a semiconductor substrate; forming a pad connected to the source; forming a first insulating layer on the resultant structure; forming bit lines connected to the drain on the

first insulating layer; forming an oxidation preventing layer on the resultant structure; forming a second insulating layer on the oxidation preventing layer; forming a contact hole exposing a portion of the pad; forming a spacer on the sidewall of the contact hole; forming a storage electrode connected to the pad via the contact hole; and sequentially forming a dielectric layer and a plate electrode on the resultant structure.

The bit lines may be formed by the sequential deposition and patterning of polysilicon and silicide, or the bit lines may be formed of other suitable conductors.

The oxidation preventing layer may be formed of a nitride layer and is preferably formed to a thickness of about 1,000 angstroms or below. The nitride layer may be formed using a low pressure chemical vapor deposition (LPCVD) process or a rapid thermal nitridation (RTN) process. The LPCVD process may be performed at a temperature of about 600 ± 100 ℃ under a pressure of about 1 torr or less using a gas mixture of dichlorosilane (SiH_2Cl_2) and ammonia (NH_3) as a reactant gas. The RTN process is preferably performed at a temperature of about 900 ± 100 ℃ under atmospheric pressure or less using an ammonia (NH_3) gas as a reactant gas.

The oxidation preventing layer may be formed by nitriding the surface of the resultant structure containing the bit lines using a gas containing nitrogen. An ammonia (NH_3) or similar gas may be used as the gas containing the nitrogen, and a plasma method, a thermal annealing method, or a rapid thermal process (RTP) may be employed.

The oxidation preventing layer may be formed to be thicker at the side walls and on top of the bit line than on the surface of the second insulating layer.

The step of forming the dielectric layer comprises the steps of depositing a nitride layer on the storage electrode, and oxidizing the semiconductor substrate having the nitride layer under a wet-oxidative atmosphere. The wet oxidation is preferably performed at a temperature of about 700~900 ℃.

According to another aspect of the present invention, there is provided a method for manufacturing a semiconductor memory device including the steps of forming a transistor including a gate, a source, and a drain in active regions of a semiconductor substrate; forming a pad connected to the source; forming a first insulating layer on the resultant structure; forming bit lines connected to the drain on the first insulating layer; forming an oxidation preventing layer on the resultant structure; forming a second insulating layer on the oxidation preventing layer; forming a contact hole exposing a portion of the pad; forming a dual spacer comprised of a nitride layer and an oxide layer on the sidewall of the contact hole; forming a storage electrode connected to the pad via the contact hole; and sequentially forming a dielectric layer and a plate electrode on the resultant structure.

The bit lines may be formed by sequentially depositing and patterning polysilicon and silicide.

The oxide layer for the dual spacer may be composed of a high temperature oxide (HTO) layer or an undoped silicate glass (USG) layer. The nitride layer and the oxide layer for the dual spacer are each preferably formed to a thickness of about 100~300 angstroms.

The step of forming the dielectric layer comprises the steps of depositing a nitride

layer on the resultant structure having the storage electrode, and oxidizing the nitride layer under a wet-oxidative atmosphere. The wet oxidation is preferably performed at a temperature of about 700~900 ℃.

According to still another aspect of the present invention, there is provided a method for manufacturing a semiconductor memory device including the steps of forming a transistor including a gate, a source, and a drain in active regions of a semiconductor substrate; forming a pad connected to the source; forming a first insulating layer on the resultant structure; forming bit lines connected to the drain on the first insulating layer; forming a second insulating layer on the resultant structure; forming a contact hole exposing a portion of the pad; forming a spacer on side walls of the contact hole; forming a storage electrode connected to the pad via the contact hole; forming an oxidation preventing layer on the resultant structure; and sequentially forming a dielectric layer and a plate electrode on the resultant structure.

The bit lines may be formed by sequentially depositing and patterning polysilicon and silicide.

The oxidation preventing layer may be formed by nitriding the surface of the resultant structure having the storage electrode using a gas containing nitrogen. A ammonia (NH_3) may be used as the gas containing the nitrogen. Also, the nitridation process may be performed using a plasma method, a thermal annealing method, or a rapid thermal process (RTP).

The step of forming the dielectric layer comprises the steps of depositing a nitride layer on the resultant structure having the storage electrode, and oxidizing the nitride

layer under a wet-oxidative atmosphere. The wet oxidation is preferably performed at a temperature of about 700~900 ℃.

According to the present invention, even if misalignment occurs in patterning a storage electrode, the bit lines may be prevented from being oxidized in the course of forming a dielectric layer. Also, this process allows the subsequent step of forming the dielectric to be performed easily.

A method for manufacturing a semiconductor memory device of the present invention will now be described with reference to the attached drawings.

<u>Embodiment 1</u>

FIGS. 4 through 7 are sectional views for explaining a method of forming a semiconductor memory device according to a first embodiment of the present invention.

FIG. 4 shows the steps of forming a transistor (not shown), a pad 42, and bit line 46 and 48.

In more detail, field oxide layers 40 divide a semiconductor substrate 200 into active regions (not shown). The field oxide is formed by a conventional isolation technology. Then, a transistor (not shown) having is formed in the active region of the semiconductor substrate 200. Polysilicon is then deposited on the resultant structure having the transistor and is patterned, thereby forming a pad 42 for connecting a storage electrode to be formed later and the active region (i.e., the source) of the semiconductor substrate 200. An insulating layer is deposited on the resultant structure and is planarized, thereby forming a first insulating layer 44 for insulating the transistor from other conductive layers. To facilitate the planarization, the first

insulating layer 44 may be formed of a borophosphosilicate glass (BPSG) layer, an undoped silicate glass (USG) layer, or another suitable insulating material.

Next, the first insulating layer 44 is partially etched to form a contact hole (not shown) exposing the drain (not shown) of the transistor. A doped polysilicon layer and a silicide layer are sequentially formed on the resultant structure and then patterned, thereby forming the bit lines 46 and 48 that are connected to the transistor drains.

FIG. 5 shows the step of forming an oxidation preventing layer 50 for preventing oxidation of the bit lines 46 and 48.

In more detail, an insulating material for preventing oxidation, e.g., a nitride layer, is deposited over the entire surface of the resultant structure comprising the first insulating layer 44 and bit lines 46 and 48, thereby forming the oxidation preventing layer 50. The oxidation preventing layer 50 serves to prevent oxidation of the bit lines 46 and 48 during a subsequent oxidation process associated with forming a dielectric layer for a capacitor. In this embodiment, the oxidation preventing layer 50 is preferably formed to be thick enough to prevent oxidation of the bit line 46 and 48, e.g., to a thickness of 1,000 angstroms or less.

FIG. 6 shows the steps of forming a contact hole 58 and forming a spacer 60.

In more detail, an insulating layer which may be easily planarized, e.g., a BPSG or USG layer, is deposited over the entire surface of the resultant structure having the oxidation preventing layer 50 and then flowed, thereby forming a second insulating layer 52. The second insulating layer 52 not only insulates the bit line 46 and 48 from other conductive layers but also planarizes the step that occurs due to the height of the bit

line 46 and 48, thereby facilitating subsequent processes. Next, a nitride layer 54 of about 500 angstroms thickness and an oxide layer 56 of about 2,000 angstroms thickness are sequentially deposited on the resultant structure.

Subsequently, the oxide layer 56, the nitride layer 54, the second insulating layer 52, and the first insulating layer 44 are sequentially anisotropically etched by photolithography, thereby forming a contact hole 58 for connecting the storage electrode to the pad 42. Next, a nitride layer having a thickness of 500 angstroms or less is deposited on the resultant structure and then anisotropically etched, thereby forming the spacer 60 at the inner side walls of the contact hole 58. The spacer 60 is for preventing the bit lines 46 and 48 from being oxidized from the sidewall of the contact hole 58 during the subsequent process of forming a dielectric layer.

FIG. 7 shows the step of forming a capacitor comprised of a storage electrode 62, a dielectric layer 64, and a plate electrode 66.

In more detail, a doped polysilicon layer is deposited to a predetermined thickness over the entire surface of the resultant structure having the spacer 60 and then anisotropically etched to form the storage electrode 62 connected to the pad 42. Subsequently, the dielectric layer 64 for a capacitor is formed. To form the dielectric layer 64, a thin nitride layer is first deposited over the entire surface of the resultant structure having the storage electrode 62. At this point, if the second insulating layer 52 on the sidewall of the contact hole is exposed by misalignment between the mask for patterning the storage electrode 62 and the contact hole 58 formed during photolithography, the nitride layer is deposited thinly on the area where the second

insulating layer 52 is exposed compared with the thickness of the nitride layer deposited the other structures. Thereafter, the nitride dielectric layer is oxidized under a wet-oxidation atmosphere at a high temperature of about 700~900 ℃, thereby forming an oxide layer on the nitride layer. In the conventional memory device, the bit lines 46 and 48 are oxidized by oxygen (O_2) diffused through a portion of the first insulating layer where the nitride layer for a dielectric layer is deposited thinly during the oxidation step. However, according to the present invention, the bit lines 46 and 48 are protected from oxidation because they are surrounded by the oxidation preventing layer 50. Finally, a doped polysilicon layer is deposited on the resultant structure having the dielectric layer 64 and then patterned, thereby forming the plate electrode 66.

<u>EMBODIMENT 2</u>

FIG. 8 is a sectional view for explaining a method for forming a semiconductor memory device according to a second embodiment of the present invention. Here, those elements which are the same as those of FIG. 7 are designated by the same reference numerals.

The first embodiment provided a method of preventing oxidation of bit lines, by depositing a thin nitride layer serving as an oxygen diffusion preventing layer, before forming an insulating layer after forming the bit lines, and depositing the insulating layer thereon. In this embodiment, provides a method of thickly depositing a nitride layer on sidewalls and top of bit lines while thinly depositing the nitride layer on the rest of the regions to facilitate subsequent processes.

If the nitride layer is deposited as an oxidation preventing layer 50 using a

LPCVD method or a RTN method after forming bit line, initial layer growth rates of the nitride layer may differ depending on the physical properties of the bit line and the insulating layer. In other words, while the nitride layer deposited on the bit lines comprising silicide and polysilicon is deposited to a desired thickness, the nitride layer is deposited more thinly on the first insulating layer 44 comprising BPSG or USG. The reason for the foregoing is that it is difficult to attain initial nucleation of the nitride layer on the BPSG layer. For example, when the nitride layer is deposited on the bit lines to a thickness of about 50 angstroms, the nitride layer is deposited on the BPSG layer to a thickness of about 10~20 angstroms.

Accordingly, when the LPCVD or RTN method is used, the nitride layer is deposited thickly on sidewalls and top of the bit lines while the nitride layer is deposited thinly on the rest of the regions, as illustrated in FIG. 8. If these methods are used, oxidation of the bit lines is effectively prevented since the bit lines 46 and 48 are surrounded by the oxidation preventing layer 50 even if misalignment occurs when patterning the storage electrode, which causes the nitride layer for a dielectric layer 64 to be deposited thinly. Also, since the oxidation preventing layer 50 is deposited thinly on the first insulating layer 44, the subsequent step of forming the contact hole for connecting the storage electrode 62 to the pad 42 can be easily performed.

If the LPCVD method is employed, the oxidation preventing layer 50 is preferably deposited under a pressure of 1 torr or less at a temperature of 600±100 ℃ using a mixed gas of dichlorosilane (SiH_2Cl_2) and ammonia (NH_3) as a reactant gas. If the RTN method is employed, the oxidation preventing layer is deposited at a temperature

of 900±100 ℃ using an ammonia (NH_3) gas as a reactant gas, and is preferably deposited under atmospheric pressure or a lower pressure.

EMBODIMENT 3

FIGS. 9 and 10 are sectional views for explaining a method of forming a semiconductor memory device according to a third embodiment of the present invention.

Referring to FIG. 9, a contact hole for connecting the storage electrode to the pad 42 is formed using the same steps in the first embodiment. Next, a nitride layer 60 and an oxide layer 75 are sequentially deposited over the entire surface of the resultant structure having the contact hole. The oxide layer 75 may be a high temperature oxide (HTO) layer or an undoped silicate glass (USG) layer. Next, the nitride layer 60 and the oxide layer 75 are anisotropically etched, thereby forming a dual spacer comprised of the nitride layer 60 and the oxide layer 75 on the sidewall of the contact hole.

Referring to FIG. 10, a storage electrode 62 connected to the pad 42, a dielectric layer 64, and a plate electrode 66 are sequentially formed on the resultant structure having the dual spacer using the same step described in the first embodiment. In the course of performing photolithography for forming the storage electrode 62 after depositing a doped polysilicon layer the contact hole may be partially exposed by misalignment, as shown in FIG. 10. However, since the spacer is formed doubly on the sidewall of the contact hole, even if an overetch is performed during the patterning of the storage electrode 62, much of the spacer formed of the nitride layer 60 is still left. That is to say, the surface of the second insulating layer 52 is not exposed by the

overetch. Thus, the oxidation of the bit lines 46 and 48 may be prevented because the nitride layer 60 forms a barrier against diffusion of oxygen into the second insulating layer 52.

In this embodiment, to prevent the oxidation of the bit line, a nitride spacer 60 of at least 50 angstroms must be left on the surface of the second insulating layer 52. In other words, even if the nitride layer is etched from the upper inner side walls of the contact hole by the misalignment generated between the storage electrode 62 and the contact hole, the oxidation of the bit line can be prevented if the thickness of the remaining nitride layer is more than 50 angstroms. Therefore, the nitride layer 60 and the oxide layer 75 for a spacer are preferably each formed to a thickness of approximately 100~300 angstroms.

EMBODIMENT 4

FIG. 11 is a sectional view for explaining a method of forming a semiconductor memory device according to a fourth embodiment of the present invention. Here, those elements which are the same as those in the first through third embodiments are designated by the same reference numerals.

Referring to FIG. 11, the same steps as those in the first through third embodiments are performed until the bit lines 46 and 48 are formed. Next, the surface of the resultant structure having the first insulating layer 44 and bit lines 46 and 48 is nitrided using a nitrogen-containing gas. As a result, a thin nitride layer 80 is formed on the surface of the resultant structure, as shown. Therefore, the same effects as in the first and second embodiments can be obtained.

Also, because the nitride layer 80 formed by nitridation is very thin, i.e., 30~50 angstroms, a nitride sill or ledge is not produced on the sidewall of the contact hole when performing subsequent processes such as a contact hole forming process in which the storage electrode and a pad are connected and a metal contact forming process.

The surface of the resultant structure having the bit lines 46 and 48 may be processed by using a plasma method, a thermal annealing method, or an RTP. A gas containing nitrogen, such as ammonia (NH_3) gas, can be used as a reactant gas.

The plasma method is preferably performed at a temperature of 200~400 ℃ for more than 1 minute. The thermal annealing method is preferably performed at a temperature of 800~900 ℃ for more than 30 minutes. The RTP is preferably performed at a temperature of 800~1000 ℃ for more than 1 minute.

EMBODIMENT 5

FIG. 12 is a sectional view for explaining a method of forming a semiconductor memory device according to a fifth embodiment of the present invention. Here, those elements which are the same as those of the first through fourth embodiments are designated by the same reference numerals.

Referring to FIG. 12, the same steps as those in the first embodiment are performed until a storage electrode 62 is formed, with the exception that the oxidation preventing layer 50 in the first embodiment is not formed. In this embodiment, if misalignment occurs when patterning the storage electrode 62, the surface of the second insulating layer 52 in the upper portion of the contact hole is exposed.

However, the surface of the resultant structure having the storage electrode 62 is nitrided using a gas containing nitrogen by the same method as in the fourth embodiment. As a result, as in the fourth embodiment, a thin nitride layer 85 having a thickness of about 30~50 angstroms is formed on the surface of the resultant structure. Thereafter, a dielectric layer 64 and a plate electrode 66 are formed.

As in the fourth embodiment, the surface of the resultant structure may be processed by using a plasma method, a thermal annealing method, or an RTP. A gas containing nitrogen, such as ammonia (NH_3) gas, may be used as a reactant gas.

When the surface of the resultant structure is nitrided after forming the storage electrode 62, the surface of the exposed second insulating layer 52 is also nitrided. Accordingly, since a nitride layer for a dielectric layer 64 is formed on nitrided underlayers during a step of forming the dielectric layer, the dielectric layer may be formed more thickly rather than being dependent on the individual properties of the different underlayers. Therefore, the nitride layer for a dielectric layer is deposited on the surface of the second insulating layer 52 as thickly as or thicker than on the surface of the storage electrode 62. Therefore, the bit line oxidation due to diffused oxygen can be prevented when the oxide layer in the dielectric is subsequently formed.

FIG. 13 is a graph for comparing the thicknesses of the nitride layers deposited on a BPSG layer before and after nitridation the surface of the BPSG layer.

In FIG. 13, ① indicates the case of omitting a surface processing, ② indicates the case of performing a plasma process at a temperature of 400 ℃ for 240 seconds using an ammonia (NH_3) gas, ③ indicates the case of performing an RTN process at a

temperature of 800 ℃ for 90 seconds, ④ indicates the case of performing an RTN process at a temperature of 1,000 ℃ for 90 seconds, and ⑤ indicates the case of performing a thermal annealing process at a temperature of 820 ℃ for 60 minutes using an ammonia (NH_3) gas.

As can be seen from FIG. 13, the nitride layer is deposited thicker in the case of depositing the same after processing the surface than in the case of omitting the surface processing. Therefore, surface processing by nitriding the surface of the storage electrode structure tends to eliminate the dependence on the underlayer of the nitride layer thickness in the dielectric layer 64, so that the nitride layer is deposited on the surface of the exposed second insulating layer (52 of FIG. 12) as thickly as or thicker than on the surface of the storage electrode (62 of FIG. 12). Therefore, the bit line oxidation due to diffused oxygen can be prevented when the oxide layer in the dielectric is subsequently formed.

Although the present invention has been described in detail through illustrative embodiments, the invention is not limited to the above-described embodiments. Various modifications may be performed by one skilled in the art within the scope and spirit of this invention.

[Effect of the Invention]

As described above, in the method for manufacturing a semiconductor memory device according to the present invention, after forming a bit line or a storage electrode, an oxidation preventing layer is formed on the resultant structure. Alternatively, a dual

spacer may be formed on the sidewall of the contact hole. Accordingly, even if misalignment occurs when patterning the storage electrode, the bit lines may be prevented from being oxidized by oxygen diffused through the sidewall of the contact hole during the formation of a dielectric layer. Particularly, by nitriding the surface of the resultant structure obtained after forming the bit lines or storage electrodes, the oxidation of the bit lines may be prevented as well as eliminating the sill on inner sidewalls of the contact hole when performing subsequent processes such as a storage electrode contact or a metal contact forming process.

What is claimed is:

1. A method for manufacturing a semiconductor memory device comprising the steps of:

forming a transistor including a gate, a source, and a drain in active regions of a semiconductor substrate;

forming a pad connected to the source on the semiconductor substrate on which the transistor is formed;

forming a first insulating layer on the entire resultant structure having the pad;

forming a plurality of bit lines connected to the drain on the first insulating layer;

forming an oxidation preventing layer over substantially the entire surface of the bit lines and the first insulating layer;

forming a second insulating layer on the oxidation preventing layer;

forming a contact hole exposing a portion of the semiconductor substrate;

forming a spacer on inner sidewalls of the contact hole;

forming a storage electrode connected to the pad via the contact hole; and

sequentially forming a dielectric layer and a plate electrode on the storage electrode.

2. The method of claim 1, wherein the bit lines are formed by sequentially stacking polysilicon and silicide and then patterning.

3. The method of claim 1, wherein the oxidation preventing layer is formed

by depositing a nitride layer on the resultant structure having the bit lines.

4. The method of claim 3, wherein the oxidation preventing layer is formed by a low pressure chemical vapor deposition (LPCVD) process or a rapid thermal nitrization (RTN).

5. The method of claim 4, wherein the LPCVD process is performed at a temperature of about 600 ± 100 ℃ under a pressure of about 1 torr or less using a gas mixture of dichlorosilane (SiH_2Cl_2) and ammonia (NH_3) as a reactant gas.

6. The method of claim 4, wherein the RTN process is performed at a temperature of about 900 ± 100 ℃ under a pressure of atmospheric pressure or less using an ammonia (NH_3) gas as a reactant gas.

7. The method of claim 1, wherein the oxidation preventing layer is formed to a thickness of about 1,000 angstroms or below.

8. The method of claim 1, wherein the oxidation preventing layer is formed by nitriding the surface of the bit lines and the first insulating layer.

9. The method of claim 8, wherein the gas containing nitrogen is an ammonia (NH_3) gas.

10. The method of claim 8, wherein the step of nitriding the surface of the bit lines and the first insulating layer using the gas containing nitrogen is performed by a plasma process, a thermal annealing process, or a rapid thermal process (RTP).

11. The method of claim 1, wherein the oxidation preventing layer is deposited thickly on sidewalls and top of the bit lines than the surface of the second insulating layer.

12. The method of claim 1, wherein the step of forming the dielectric layer comprises:

depositing a nitride layer on the resultant structure having the storage electrode;

oxidizing the nitride layer under a wet-oxidative atmosphere.

13. The method of claim 12, wherein the wet oxidation is performed at a temperature of about 700~900 ℃.

14. A method for manufacturing a semiconductor memory device comprising the steps of:

forming a transistor including a gate, a source, and a drain in active regions of a semiconductor substrate;

forming a pad connected to the source on the semiconductor substrate on which the transistor is formed;

forming a first insulating layer on the resultant structure having the pad;

forming a plurality of bit lines connected to the drain on the first insulating layer;

forming a second insulating layer on the resultant structure having the bit lines;

forming a contact hole exposing a portion of the semiconductor substrate;

forming a dual spacer comprised of a nitride layer and an oxide layer on the sidewall of the contact hole; forming a storage electrode connected to the pad via the contact hole;

forming a storage electrode connected to the pad via the contact hole; and

sequentially forming a dielectric layer and a plate electrode on the storage electrode.

15. The method of claim 14, wherein the bit lines are formed by sequentially stacking and patterning polysilicon and silicide.

16. The method of claim 14, wherein the oxide layer for the dual spacer is composed of a high temperature oxide (HTO) layer or an undoped silicate glass (USG) layer.

17. The method of claim 14, wherein the nitride layer and the oxide layer for the dual spacer are each formed to a thickness of about 100~300 angstroms.

18. The method of claim 14, wherein the step of forming the dielectric layer comprises:

depositing a nitride layer on the resultant structure having the storage electrode; and

oxidizing the nitride layer under a wet-oxidative atmosphere.

19. The method of claim 18, wherein the wet oxidation is performed at a temperature of about 700~900 ℃.

20. A method for manufacturing a semiconductor memory device comprising:

forming a transistor including a gate, a source, and a drain in active regions of a semiconductor substrate;

forming a pad connected to the source on the semiconductor substrate having the transistor;

forming a first insulating layer on the resultant structure having the pad;

forming bit lines connected to the drain on the first insulating layer;

forming a second insulating layer on the resultant structure having the bit lines;

forming a contact hole exposing a portion of the pad;

forming a spacer on side walls of the contact hole;

forming a storage electrode connected to the pad via the contact hole;

forming an oxidation preventing layer on the resultant structure having the storage electrode; and

sequentially forming a dielectric layer and a plate electrode on the resultant structure having the oxidation preventing layer.

21. The method of claim 20, wherein the bit lines are formed by sequentially depositing and patterning polysilicon and silicide.

22. The method of claim 20, wherein the oxidation preventing layer is formed by nitriding the surface of the resultant structure having the storage electrode using a gas containing nitrogen.

23. The method of claim 22, wherein the gas containing the nitrogen is an ammonia (NH_3) gas.

24. The method of claim 22, wherein the nitridation process is performed using a plasma method, a thermal annealing method, or a rapid thermal process (RTP).

25. The method of claim 20, wherein the step of forming the dielectric layer comprises:

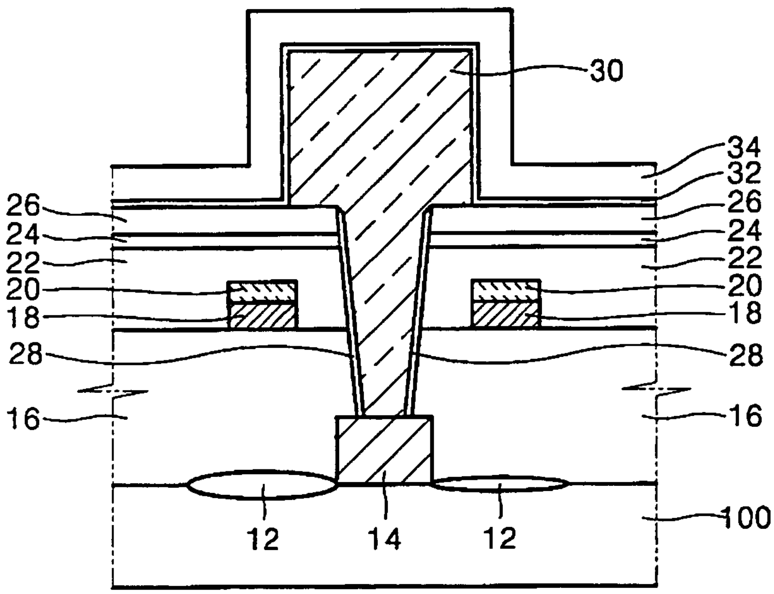
depositing a nitride layer on the resultant structure having the storage electrode;

and

oxidizing the nitride layer under a wet-oxidative atmosphere.

26. The method of claim 25, wherein the wet oxidation is performed at a temperature of about 700~900 ℃.

FIG. 1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20
18
28
16
26
24
22
20
18
28
16
12
14
12
100

FIG. 2

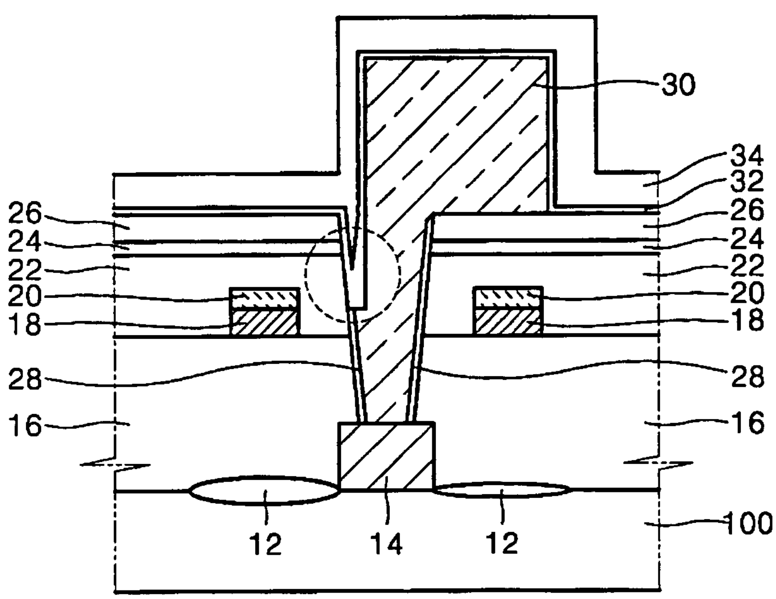

30
34
32
26
24
22
20
18
28
16
26
24
22
20
18
28
16
12
14
12
100

FIG. 3

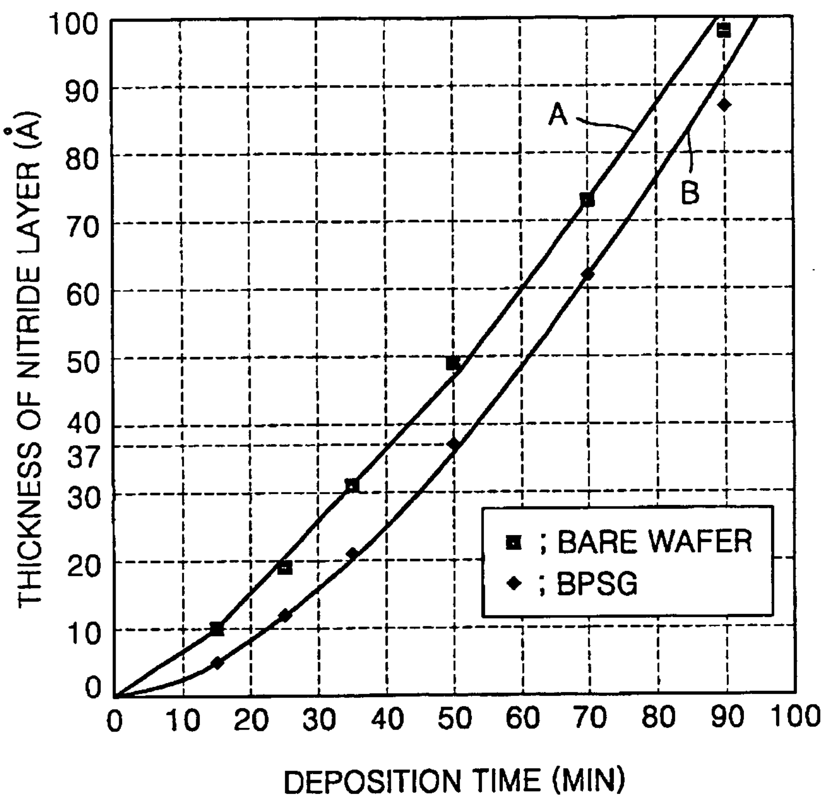

100
90
80
70
60
50
40
37
30
20
10
0
THICKNESS OF NITRIDE LAYER (Å)
0 10 20 30 40 50 60 70 80 90 100
DEPOSITION TIME (MIN)
A
B
; BARE WAFER
; BPSG

FIG. 4

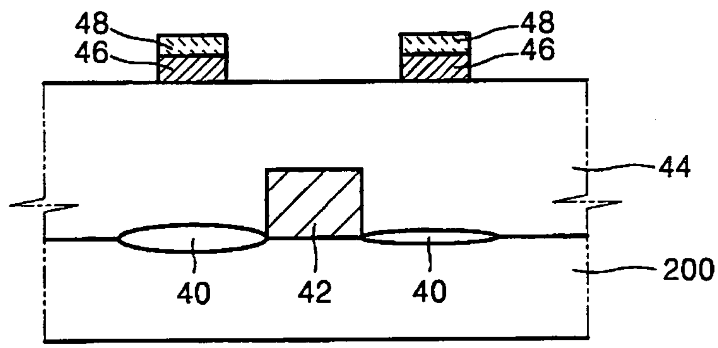


FIG. 5

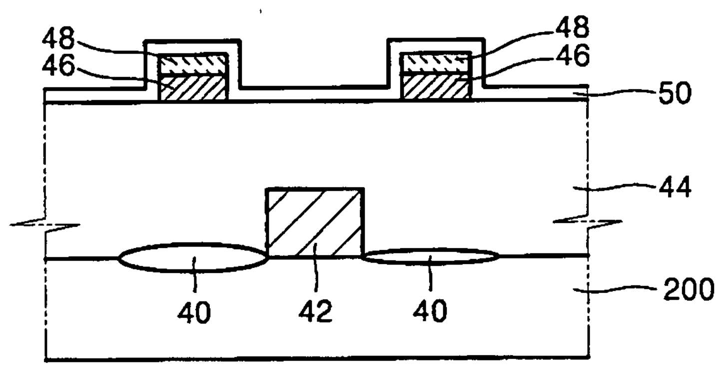


FIG. 6

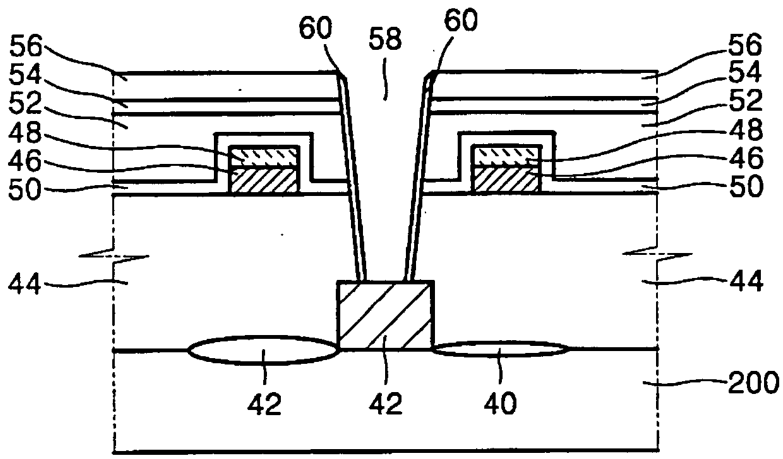

56
54
52
48
46
50
44
60
58
60
56
54
52
48
46
50
44
42
42
40
200

FIG. 7

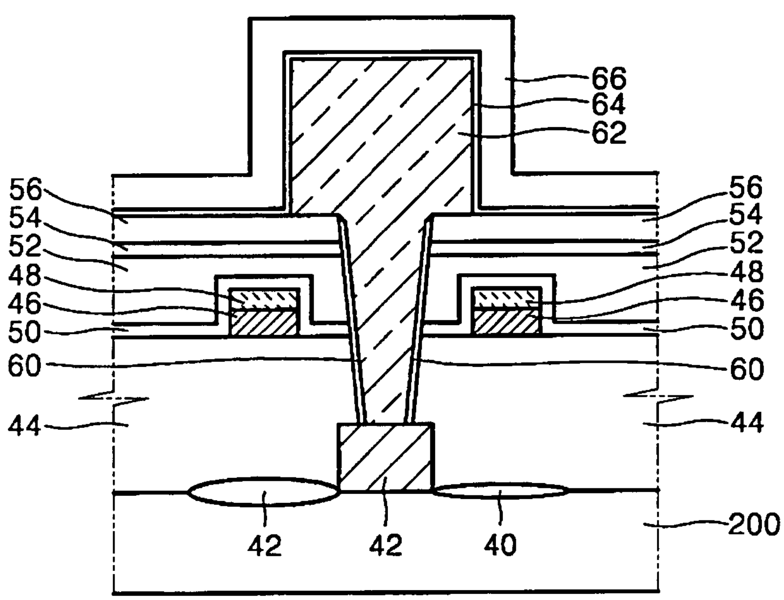

66
64
62
56
54
52
48
46
50
60
44
56
54
52
48
46
50
60
44
42
42
40
200

FIG. 8

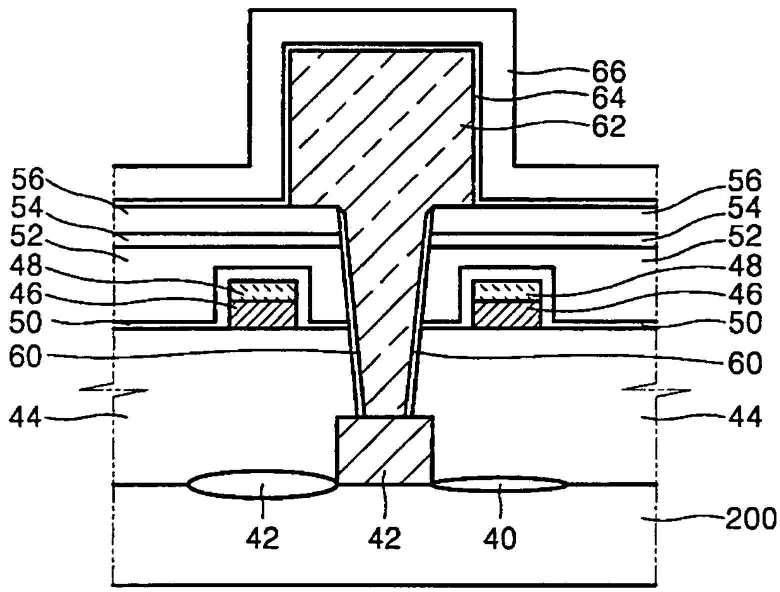

66
64
62
56
54
52
48
46
50
60
44
42
42
40
200

FIG. 9

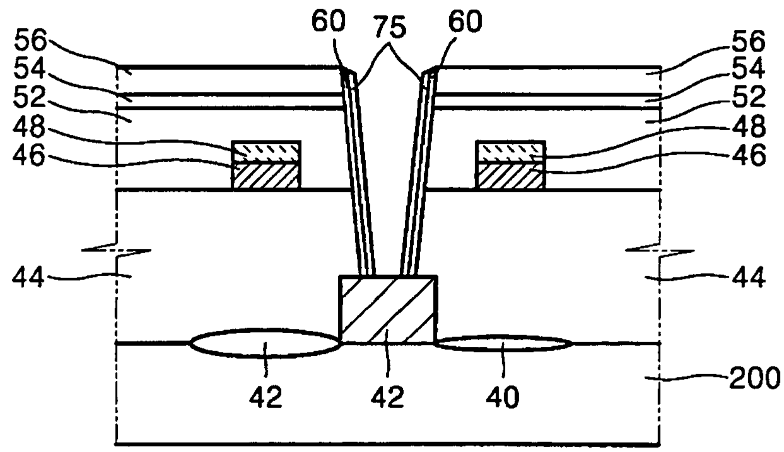

60
75
60
56
54
52
48
46
44
42
42
40
200

FIG. 10

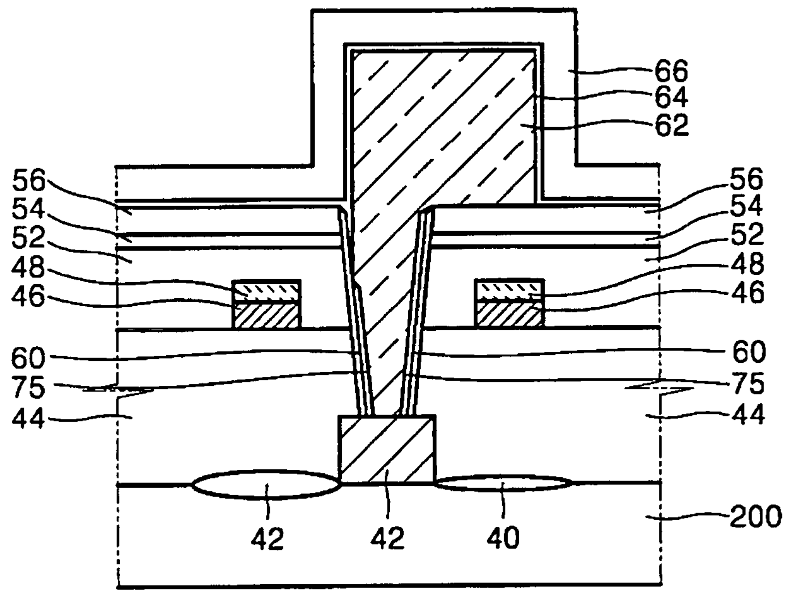

66
64
62
56
54
52
48
46
60
75
44
56
54
52
48
46
60
75
44
42
42
40
200

FIG. 11

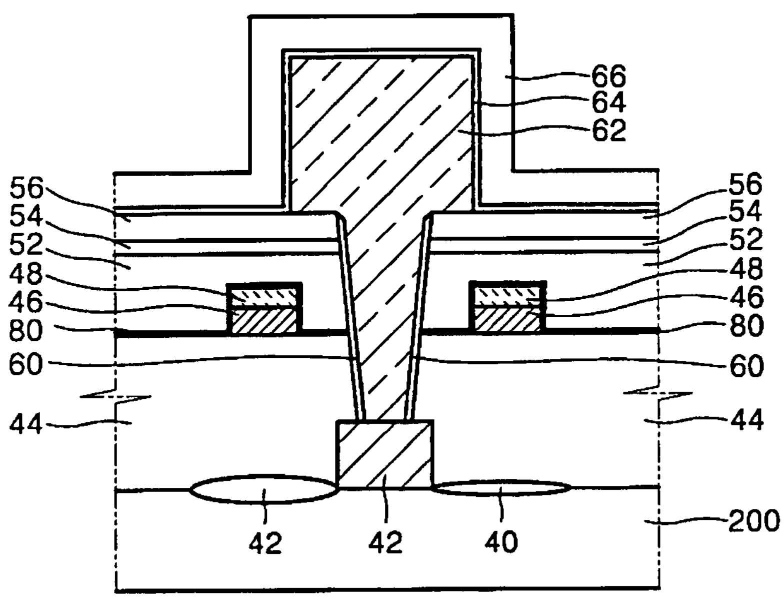

66
64
62
56
54
52
48
46
80
60
44
56
54
52
48
46
80
60
44
42
42
40
200

FIG. 12

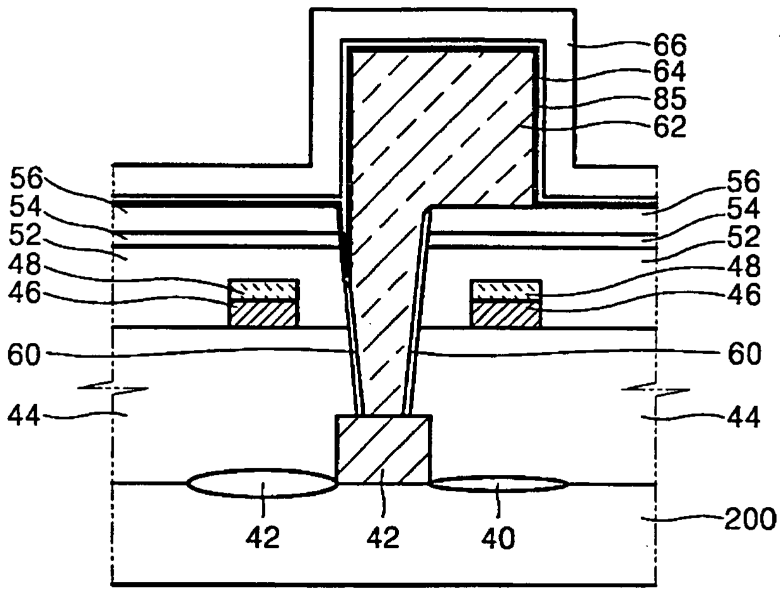
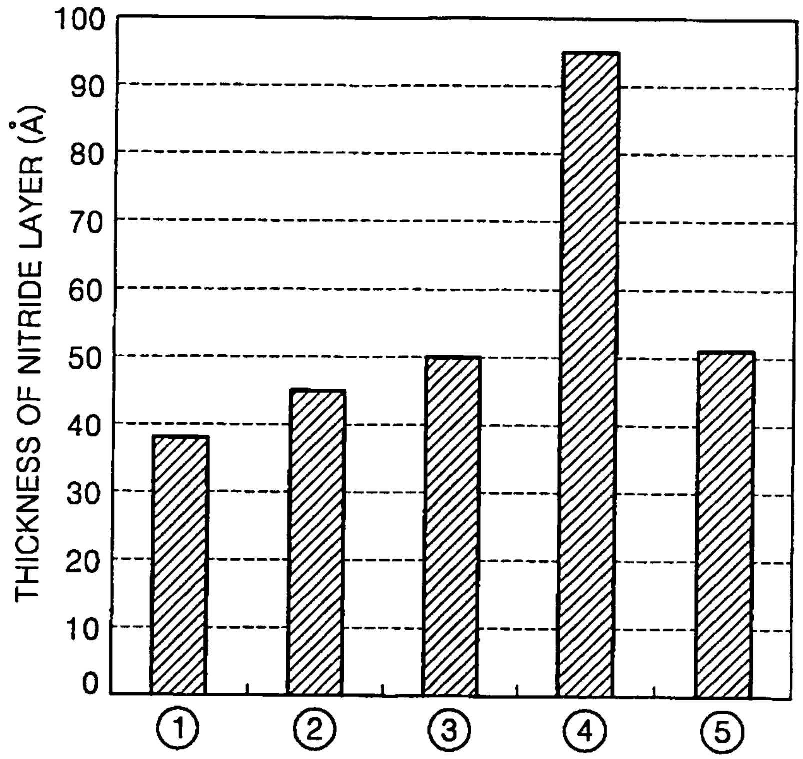


FIG. 13



THICKNESS OF NITRIDE LAYER (Å)
100
90
80
70
60
50
40
30
20
10
0
①
②
③
④
⑤